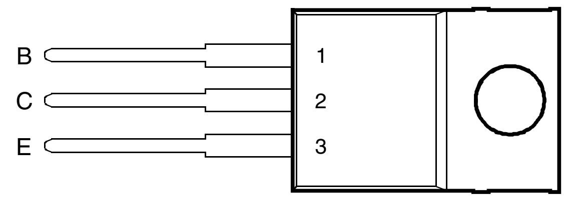
BUL791
NPN SILICON POWER TRANSISTOR

- **Designed Specifically for High Frequency Electronic Ballasts up to 125 W**
- **h_{FE} 6 to 22 at V_{CE} = 1 V, I_C = 2 A**
- **Low Power Losses (On-state and Switching)**
- **Key Parameters Characterised at High Temperature**
- **Tight and Reproducible Parametric Distributions**

TO-220 PACKAGE
(TOP VIEW)



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Collector-emitter voltage (V_{BE} = 0)	V_{CES}	700	V
Collector-base voltage (I_E = 0)	V_{CBO}	700	V
Collector-emitter voltage (I_B = 0)	V_{CEO}	400	V
Emitter-base voltage	V_{EBO}	9	V
Continuous collector current	I_C	4	A
Peak collector current (see Note 1)	I_{CM}	8	A
Peak collector current (see Note 2)	I_{CM}	14	A
Continuous base current	I_B	2.5	A
Peak base current (see Note 2)	I_{BM}	3.5	A
Continuous device dissipation at (or below) 25°C case temperature	P_{tot}	75	W
Operating junction temperature range	T_j	-65 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. This value applies for t_p = 10 ms, duty cycle ≤ 2%.
2. This value applies for t_p = 300 µs, duty cycle ≤ 2%.

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electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{CEO(sus)}$	Collector-emitter sustaining voltage	I_C = 100 mA	L = 25 mH	(see Note 3)	400			V
I_{CES}	Collector-emitter cut-off current	V_{CE} = 700 V V_{CE} = 700 V	V_{BE} = 0 V_{BE} = 0	 T_C = 90°C			10 200	µA
I_{EBO}	Emitter cut-off current	V_{EB} = 9 V	I_C = 0				1	mA
$V_{BE(sat)}$	Base-emitter saturation voltage	I_B = 400 mA I_B = 400 mA	I_C = 2 A I_C = 2 A	(see Notes 4 and 5) T_C = 90°C		0.94 0.86	1	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 400 mA I_B = 400 mA	I_C = 2 A I_C = 2 A	(see Notes 4 and 5) T_C = 90°C		0.25 0.3	0.4	V
h_{FE}	Forward current transfer ratio	V_{CE} = 1 V V_{CE} = 1 V V_{CE} = 5 V	I_C = 10 mA I_C = 2 A I_C = 8 A		10 6 2	16.5 12 6.5	 22 14	
V_{FCB}	Collector-base forward bias diode voltage	I_{CB} = 60 mA				850		mV

NOTES: 3. Inductive loop switching measurement.
4. These parameters must be measured using pulse techniques, t_p = 300 µs, duty cycle ≤ 2%.
5. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts, and located within 3.2 mm from the device body.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance			62.5	°C/W
$R_{\theta JC}$	Junction to case thermal resistance			1.66	°C/W

inductive-load switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{sv}	Storage time	I_C = 2 A	$I_{B(on)}$ = 400 mA	V_{CC} = 40 V		2.2	3	µs
t_{fi}	Current fall time	L = 1 mH	$I_{B(off)}$ = 800 mA	V_{CLAMP} = 300 V		95	180	ns
t_{xo}	Cross over time					210	300	ns
t_{sv}	Storage time	I_C = 2 A	$I_{B(on)}$ = 400 mA	V_{CC} = 40 V		4	6	µs
t_{fi}	Current fall time	L = 1 mH	$I_{B(off)}$ = 250 mA	V_{CLAMP} = 300 V		120	230	ns

resistive-load switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{sv}	Storage time	I_C = 2 A	$I_{B(on)}$ = 400 mA		2.2	3	µs
t_{fi}	Current fall time	V_{CC} = 300 V	$I_{B(off)}$ = 400 mA		160	250	ns

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TYPICAL CHARACTERISTICS

FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

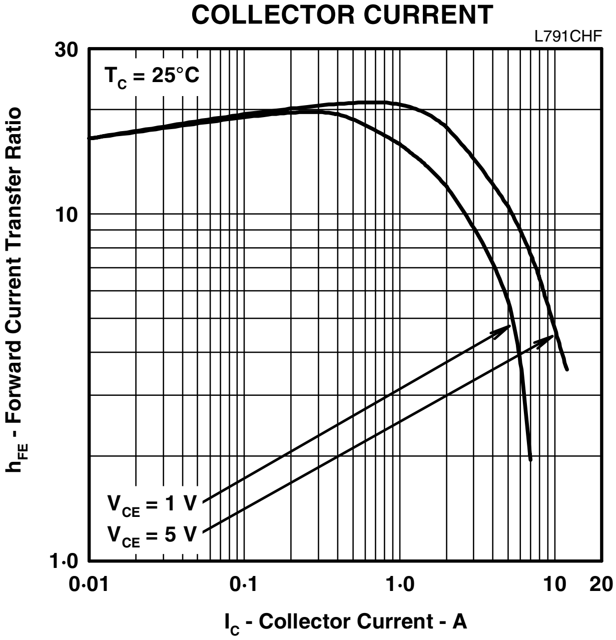

Figure 1.

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

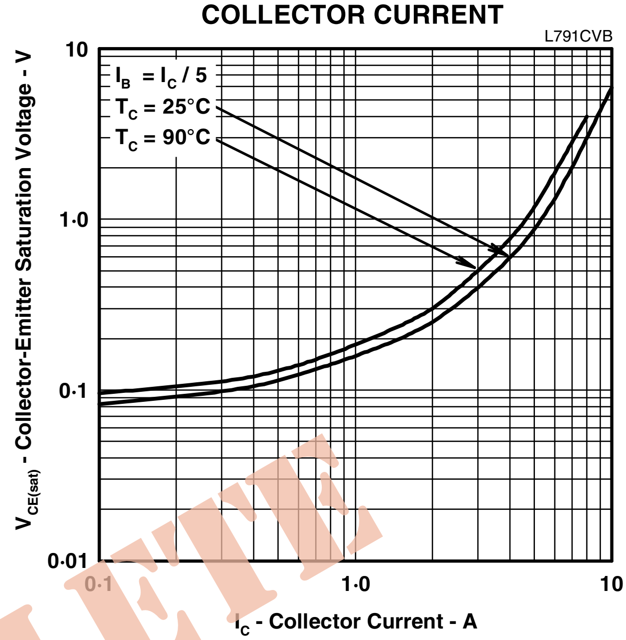

Figure 2.

INDUCTIVE SWITCHING TIMES vs COLLECTOR CURRENT

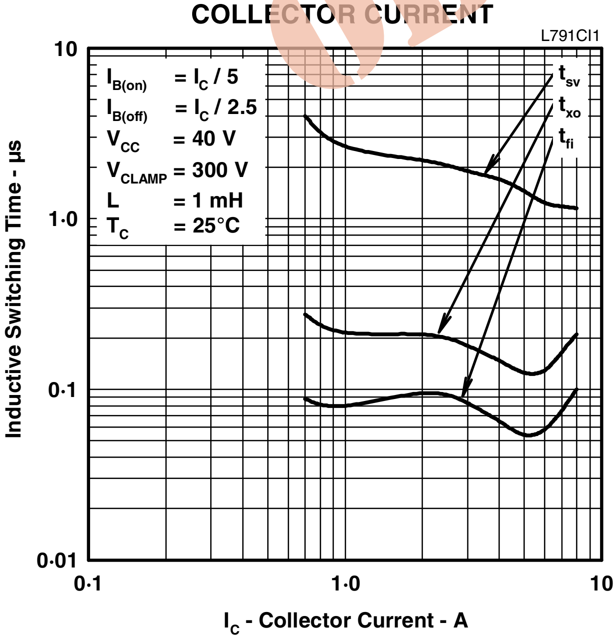

Figure 3.

INDUCTIVE SWITCHING TIMES vs CASE TEMPERATURE

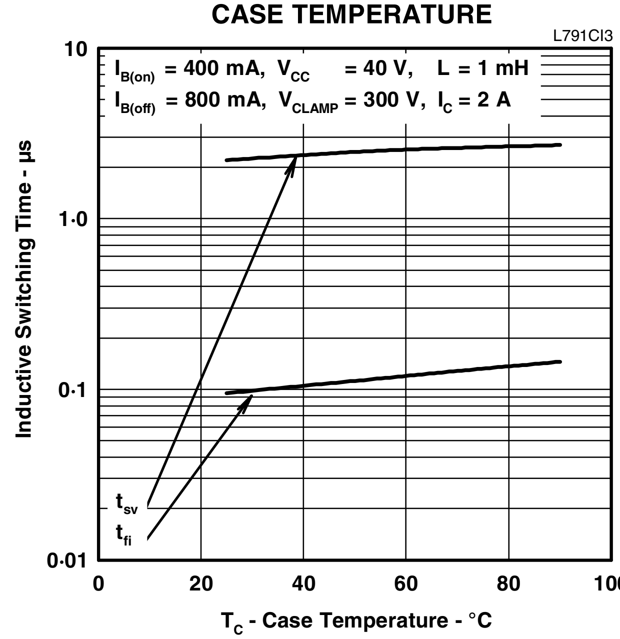

Figure 4.

TYPICAL CHARACTERISTICS

INDUCTIVE SWITCHING TIMES vs COLLECTOR CURRENT

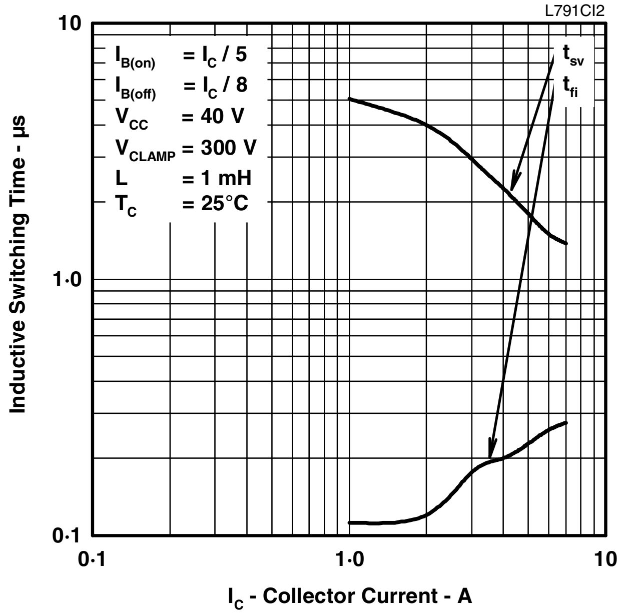

Figure 5.

INDUCTIVE SWITCHING TIMES vs CASE TEMPERATURE

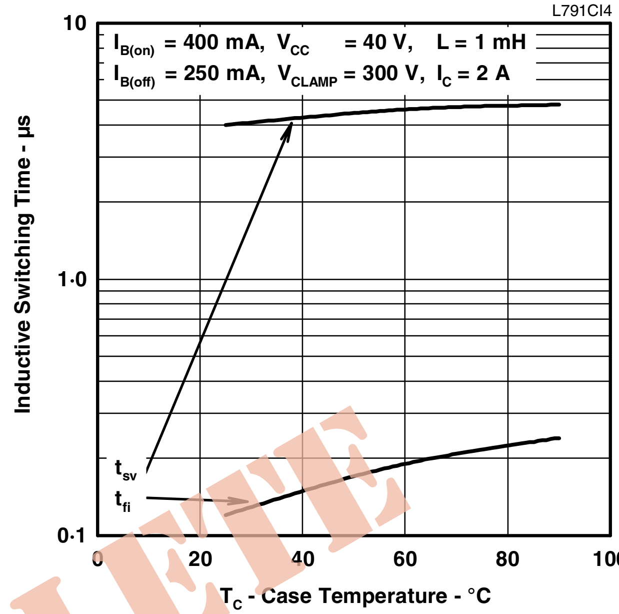

Figure 6.

RESISTIVE SWITCHING TIMES vs COLLECTOR CURRENT

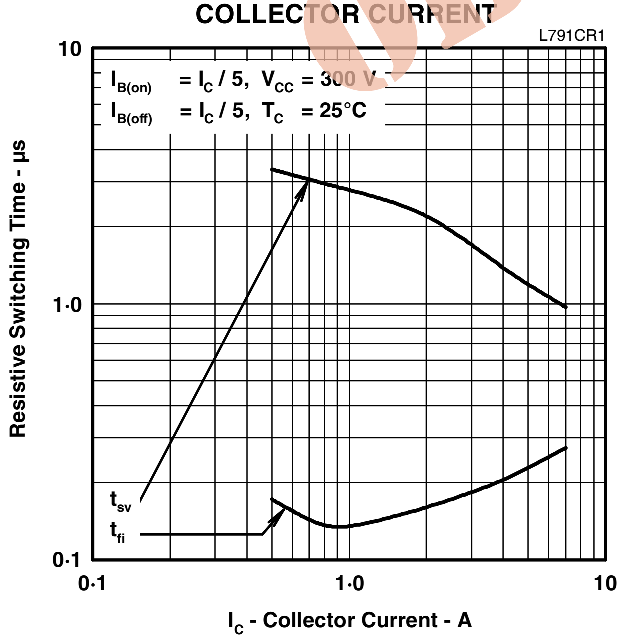

Figure 7.

RESISTIVE SWITCHING TIMES vs CASE TEMPERATURE

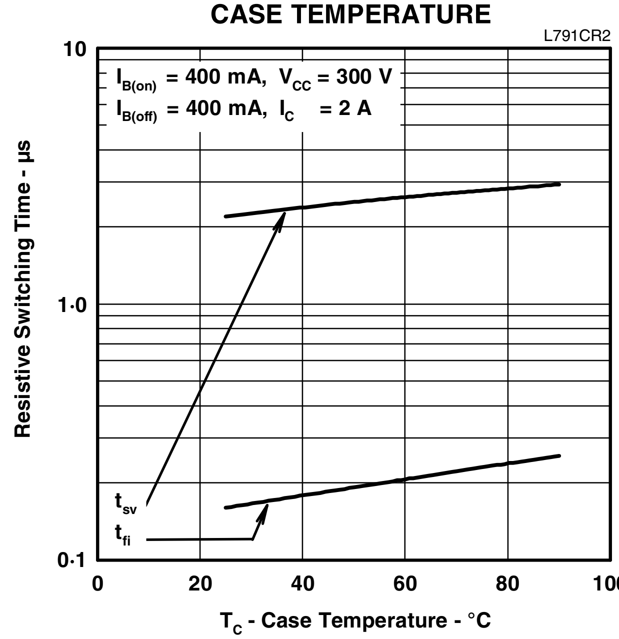

Figure 8.

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MAXIMUM SAFE OPERATING REGIONS

MAXIMUM FORWARD-BIAS SAFE OPERATING AREA

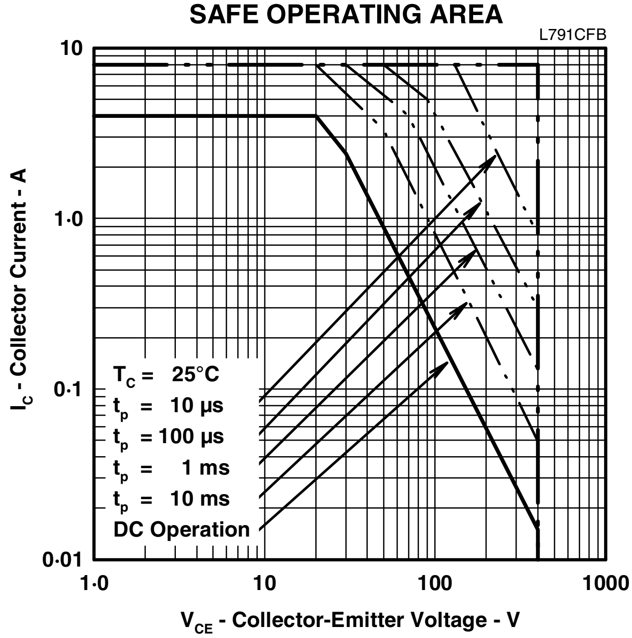

Figure 9.

MAXIMUM REVERSE-BIAS SAFE OPERATING AREA

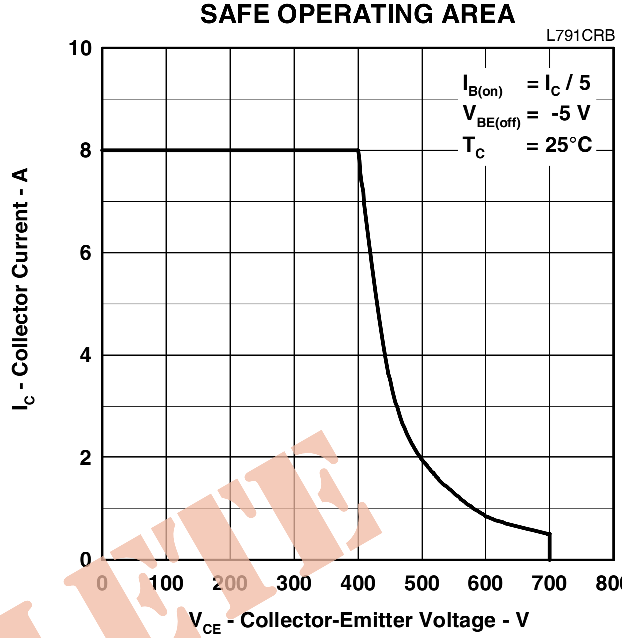

Figure 10.